WHAT IS CLAIMED IS:

1. A manufacturing method of a contact structure of a wire comprising steps of:

forming a wire on a substrate;

forming a inter-layer reaction layer on the wire by executing annealing process; and

forming a conductive layer electrically connected to the wire via the inter-layer reaction layer.

2. The method of claim 1, wherein the wire is made of a conductive material including aluminum-based material.

3. The method of claim 1, further comprising the step of forming an insulating layer having a contact hole between the wire and the conductive layer.

4. The method of claim 3, wherein the annealing process is executed before forming the insulating layer.

5. The method of claim 3, wherein the annealing process is executed after forming the insulating layer.

6. The method of claim 1, wherein the inter-layer reaction layer includes silicon or transition metal.

7. The method of claim 3, wherein the inter-layer reaction layer is inter-metallic compound layer.

8. The method of claim 1, wherein the conductive layer is made of a transparent conductive material of indium zinc oxide.

9. The method of claim 1, wherein the annealing process is executed in the range of 200-400℃.

10. A contact structure of a wire comprising:

a wire of a conductive material on a substrate;

an inter-layer reaction layer formed on the wire and including at least silicon or transition metal; and

a conductive layer electrically connected to the wire via the inter-reaction layer.

11. The contact structure of claim 10, wherein the wire is made of a conductive material including aluminum-based material.

12. The contact structure of claim 11, wherein the inter-layer reaction layer includes at least Al_XSi_X.

13. The contact structure of claim 10, wherein the inter-layer reaction layer is inter-metallic compound layer.

14. The contact structure of claim 10, wherein the conductive layer is made of a transparent conductive material of indium zinc oxide.

15. The contact structure of claim 10, further comprising an insulating layer having a contact hole exposing the inter-layer reaction layer between the wire and the conductive layer.

16. A manufacturing method of a thin film transistor array panel comprising steps of:

forming a gate wire;

forming a data wire;

forming a semiconductor layer;

forming an inter-layer reaction layer on the gate wire and the data wire through annealing process; and

forming a conductive layer electrically connected to the gate wire or the data wire via the inter-layer reaction layer.

17. The method of claim 16, further comprising the step of forming an insulating layer having a contact hole on the gate or the data wires between the gate or the data wires and the conductive layer.

18. The method of claim 16, wherein the gate wire and the data wire include a conductive material of aluminum-based material.

19. The method of claim 16, wherein the inter-layer reaction layer includes silicon or transition metal.

20. The method of claim 19, wherein the inter-layer reaction layer includes amorphous or doped amorphous silicon.

21. The method of claim 19, wherein the inter-layer reaction layer is an inter-metallic compound.

22. The method of claim 16, wherein the conductive layer is made of indium zinc oxide.

23. The method of claim 16, wherein the annealing process is executed before forming the insulating layer.

24. The method of claim 16, wherein the annealing process is executed after forming the insulating layer.

25. The method of claim 16, wherein the insulating layer is deposited in

the range of 200-400℃.

26. The method of claim 16, further comprising the step of executing a wet cleaning process using etchant or a dry cleaning process using plasma before forming the inter-layer reaction layer.

27. A manufacturing method of a thin film transistor array panel for a liquid crystal display comprising steps of:

forming a gate wire including a gate line, and a gate electrode connected to the gate line by depositing and patterning a first conductive material on an insulating substrate;

depositing a gate insulating layer;

forming a semiconductor layer;

forming a data wire including a data line intersecting the gate line, a source electrode connected to the data line and adjacent to the gate electrode and a drain electrode opposite of the source electrode with respect to the gate electrode by depositing and patterning a second conductive material;

depositing a passivation layer;

forming an inter-layer reaction layer on the gate wire and the data wire by executing annealing process;

patterning the passivation layer to form a first contact hole exposing the drain electrode; and

forming a pixel electrode electrically connected to the drain electrode through the first contact hole on the passivation layer.

28. The method of claim 27, wherein the first and the second conductive

material include a metal of aluminum-based material.

29. The method of claim 27, wherein the annealing process is executed before forming the gate insulating layer or the passivation layer.

30. The method of claim 27, wherein the annealing process is executed after forming the first contact hole.

31. The method of claim 27, wherein the pixel electrode is made of a transparent conductive material.

32. The method of claim 31, wherein the pixel electrode is made of indium zinc oxide.

33. The method of claim 27, wherein the annealing process is executed in the range of 200-400℃.

34. The method of claim 27, wherein the inter-layer reaction layer includes silicon or transition metal.

35. The method of claim 34, wherein the inter-layer reaction layer includes amorphous or doped amorphous silicon.

36. The method of claim 34, wherein the inter-layer reaction layer is an inter-metallic compound.

37. The method of claim 27, wherein the gate wire further includes a gate pad which is connected to the gate line and receives a signal from an external circuit, and the data wire further includes a data pad which is connected to the data line and receives a signal from a external circuit, and the passivation layer and the gate insulating layer have a second contact hole and a third contact hole respectively exposing the inter-layer reaction layer on the

gate pad and the data pad, and

further comprising the step of forming a redundant gate pad and a redundant data pad which are made of the same layer as the pixel electrode and respectively electrically connected to the gate pad and the data pad through the second and the third contact holes.

38. The method of claim 27, wherein the data wire and the semiconductor layer are together formed by photolithography process using a photoresist pattern having different thicknesses depending the positions.

39. The method of claim 38, wherein the photoresist pattern has a first portion having a first thickness, a second portion having a second thickness larger than the first portion, and a third portion having a third thickness smaller than the first thickness.

40. The method of claim 39, wherein a mask used for forming the photoresist pattern has a first, a second, and a third part, a transmittance of the third part is higher than the first and the second parts, a transmittance of the first part is higher than the second part.

41. The method of claim 40, wherein the first and the second portion of the photoresist pattern are respectively aligned on portion between the source electrode and the drain electrode, and the data wire.

42. The method of claim 41, wherein the first part of the mask includes a partially transparent layer, or a slit pattern smaller than the resolution of the exposure used in the exposing step, to regulate the transmittance of the first part.

43. The method of claim 27, further comprising step of :

depositing an ohmic contact layer between the data wire and the semiconductor layer.

44. The method of claim 43, wherein the data wire, the ohmic contact layer, and the semiconductor layer are formed in the same photolithography process.

45. A thin film transistor array panel comprising:

a gate wire made of a first conductive material on an insulating substrate;

a gate insulating layer covering the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire made of a second conductive material on the gate insulating layer and the semiconductor layer;

a passivation layer covering the data wire;

an inter-layer reaction layer formed on the gate wire and the data wire; and

a transparent conductive layer pattern electrically connected to the gate wire or the data wire through a first contact hole of the gate insulating layer or the passivation layer via the first contact hole.

46. The thin film transistor array panel of claim 45, wherein the first and the second conductive material include a metal of aluminum-based material.

47. The thin film transistor array panel of claim 45, wherein the insulating layer and the passivation layer are made of silicon-nitride.

48. The thin film transistor array panel of claim 45, wherein the

transparent conductive layer pattern is made of indium zinc oxide.

49. The thin film transistor array panel of claim 45, wherein the gate wire includes a gate line, a gate electrode connected to the gate line, and a gate pad which is connected to the gate line and receives a signal from an external circuit, and the data wire includes a data line, a source electrode connected to the data line, a drain electrode which is separated from the drain electrode and opposite to the drain electrode with the respect to the gate electrode, and a data pad which is connected to the data line and receives a signal from a external circuit.

50. The thin film transistor array panel of claim 45, wherein the inter-layer reaction layer includes silicon or transition metal.